



IFW

PATENT
Docket No. INTEL/18496

IN THE UNITED STATES PATENT
AND TRADEMARK OFFICE

Applicants: **SHI, et al.**

U.S. Serial No.: 10/791,004

For: "Apparatus and Method for
Performing Generational Escape
Analysis in Managed Runtime
Environments"

Filed: 3/2/2004

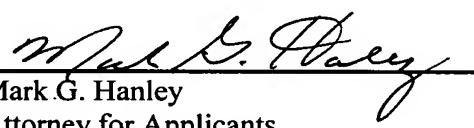
Assignee: Intel Corporation

Group Art Unit: 2122

Examiner: Unknown

) I hereby certify that this paper and the
) documents referred to as enclosed
) therewith are being deposited with the
) United States Postal Service as first
) class mail, postage prepaid, in an
) envelope addressed to Commissioner
) for Patents, P.O. Box 1450,
) Alexandria, Virginia 22313-1450 on
) this date:

) **March 16, 2005**

) 
) Mark G. Hanley
) Attorney for Applicants
) Registration No. 44,736

STATUS LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

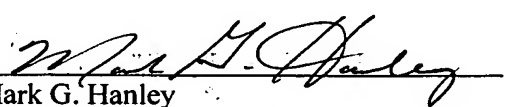
Kindly advise when an Office action can be expected in the above-referenced
matter. Please note that it has been more than three months since the last communication.

Respectfully submitted,

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March 16, 2005

By:


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Registration No.: 44,736

Attorneys for Intel Corporation